

Applicant: Christophe J. Chevallier

Title: SUPPLY VOLTAGE REDUCTION CIRCUIT FOR INTEGRATED CIRCUIT

Docket No.: 703.019US3

Serial No.: 09/955270

Filed: September 18, 2001

Due Date: July 9, 2003

Examiner: Edward Wojciechowicz

Group Art Unit: 2816

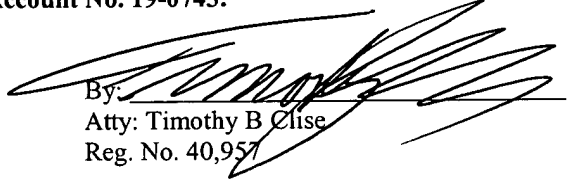
Commissioner for Patents
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We are transmitting herewith the following attached ~~papers~~ indicated with an "X"):

- ☒ A return postcard.
☒ An Amendment and Response (18 Pages).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 9th day of July, 2003.

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